

AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (currently amended) A method for forming fine gate electrodes of a semiconductor device, the method comprising:
 - forming a gate insulation layer over a semiconductor wafer;
 - forming a conductive layer over the gate insulation layer;
 - forming a low-dielectric layer over the conductive layer;
 - forming a photoresist pattern whose width linewidth is equal to the exposure limit on the low-dielectric layer;
 - patterning the low-dielectric layer using the photoresist pattern as a mask;
 - removing the photoresist pattern and shrinking the low-dielectric pattern,
a so that the shrunken low-dielectric pattern has a linewidth smaller than that of the photoresist pattern, wherein removing the photoresist pattern and shrinking the low-dielectric pattern are performed at the same time; and
 - forming fine gate electrodes by patterning the conductive layer and the gate insulation layer using the shrunken low-dielectric pattern as a mask.

2. (canceled)

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3. (previously presented) The method of claim 1, wherein forming the low-dielectric layer comprises:

depositing a low-dielectric layer over the conductive layer for the gate electrodes; and

soft-baking the low-dielectric layer at a predetermined temperature.

4. (original) The method of claim 1, wherein shrinking the low-dielectric pattern includes curing the low-dielectric pattern at a temperature of 400-500°C.

5-10. (canceled)

11. (currently amended) A method for forming fine gate electrodes of a semiconductor device, the method comprising:

forming a gate insulation layer over a semiconductor wafer;

forming a conductive layer over the gate insulation layer;

forming a low-dielectric layer over the conductive layer;

soft-baking the low-dielectric layer at a predetermined temperature;

forming a photoresist pattern whose ~~width~~ linewidth is equal to the exposure limit on the low-dielectric layer;

patterning the low-dielectric layer using the photoresist pattern as a mask;

removing the photoresist pattern;

shrinking the low-dielectric pattern ~~after the removal of the photoresist-pattern~~ so that the shrunken low-dielectric pattern has a linewidth smaller than that of the photoresist pattern; and

forming fine gate electrodes by patterning the conductive layer and the gate insulation layer using the shrunken low-dielectric pattern as a mask.

12. (previously presented) The method of claim 11, wherein forming the low-dielectric layer comprises:

depositing a low-dielectric layer over the conductive layer for the gate electrodes.

13. (previously presented) The method of claim 11, wherein shrinking the low-dielectric pattern includes curing the low-dielectric pattern at a temperature of 400-500°C.

14. (previously presented) The method of claim 11, wherein the low-dielectric layer is formed of an organic spin-on-glass layer.

15. (currently amended) The method of claim 14, wherein the organic spin-on-glass layer comprises ~~siloxanis~~ siloxanes or ~~silicesquinexanis~~ silsesquioxanes.

16. (previously presented) The method of claim 11, wherein the low-dielectric layer is formed of an inorganic spin-on-glass layer.

17. (currently amended) The method of claim 16, wherein the ~~organic~~
inorganic spin-on-glass layer comprises silicate, hydrogen silicate, or hydrogen
~~silicesquinoxane~~ silsesquioxanes.

18. (previously presented) The method of claim 1, wherein the low-dielectric
layer is formed of an organic spin-on-glass layer.

19. (currently amended) The method of claim 18, wherein the organic spin-
on-glass layer comprises ~~siloxanis~~ siloxanes or ~~silicesquinoxanis~~ silsesquioxanes.

20. (previously presented) The method of claim 1, wherein the low-dielectric
layer is formed of an inorganic spin-on-glass layer.

21. (currently amended) The method of claim 20, wherein the ~~organic~~
inorganic spin-on-glass layer comprises silicate, hydrogen silicate, or hydrogen
~~silicesquinoxane~~ silsesquioxanes.